AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0020] with the following replacement paragraph:

FIG. 1 illustrates, as an example, a block diagram of a Computer System **100**. A Bus **106** serves as main communication artery for various devices or components in the Computer System **100** to communicate with one another through information transfers. Among these devices are a Central Processing Unit (CPU) **101**, a Memory Controller **103** managing access to a Memory **102**, a Peripheral Controller Interface (I/F) **108** managing and facilitating communications **110** with a Peripheral **109**, an Ethernet I/F **111** managing and facilitating communications with other devices on a local area or other network, and a Direct Memory Access (DMA) Controller **114**.

Please replace paragraph [0025] with the following replacement paragraph:

Referring now to **FIG. 2**, a Two-Entry Buffer **202** is provided to store two successive words of information that are to be transferred from the CPU **101** to the Bus **106**. The advantage of having the first entry to the Buffer **202** is so that the CPU **101** doesn't have to wait for the Bus **106** to become available if it is busy at the time that the CPU **101** initiates a transfer of information to the Bus **106**. With the assistance of Control Logic **201**, the CPU **101** can write information to be transferred to the Bus **106** into the Buffer ~~201~~ **202** regardless of whether the Bus **106** is busy or not, and the Control Logic ~~202~~ **201** manages subsequent transfer of the written information from the Buffer **202** to the Bus **106** when the Bus **106** is available.